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10/080,913	02/21/2002	Luu Thanh Nguyen	NSC1P131X1	1176

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/080,913	NGUYEN ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-26,28-32 and 34-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-26,28-32 and 34-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/29/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The 35 USC § 112 claim rejection has been overcome by the amendment to the claims and therefore is withdrawn.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/28/08 has been entered.

Response to Arguments

Applicant's arguments filed 5/28/08 have been fully considered but they are not persuasive. Three arguments were presented with respect to the rejection of the claims.

The first argument is that Chung teaches a solid perform underfill and therefore it can't conformally surround the solder bumps.

Please note that Chung teaches the solid perform has a flow characteristic that, under heat and pressure, cause the preform to melt and flow so that it can be cured (9,

6+ & 11, 23+). This would also cause it to conformally surround the solder bumps (see Figure 5).

The second argument is that neither Chung nor Capote teaches a dam. With respect to Chung, one wouldn't be required because the underfill is supplied as a solid perform.

Please note that the rejection notes that a dam isn't taught by either Chung or Capote. The rejection says that a dam is conventionally known in the art. A dam is conventionally used to control the flow of a material. As to the lack of a need for one in Chung, please note that the flow characteristic noted above would allow for the need for a dam to control the flow of the solid preform underfill.

The final argument is that Capote doesn't teach a B-stage underfill.

Please note that the rejection addresses this on page 8 by stating that the use a B-stage underfill is conventionally known in the art.

Rejections over Chung, US Patent 6,399,178

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-26, and 35-38 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chung, US Patent 6,399,178.

Claims 19-26, and 35-38 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chung, US Patent 6,399,178.

Chung (figures 5 & 6) teaches an apparatus, comprising:

a flip chip integrated circuit [30] having flip chip bond pads [32] with solder bumps [34] formed directly on an active surface of the flip chip; and

a substantially uniform layer of B-staged underfill adhesive [12] that is partially cured and reflowable (8, 46-52), the B-staged underfill adhesive being applied directly on the active surface of the flip chip integrated circuit and around the solder bumps formed onto the active surface, the substantially uniform layer of underfill adhesive and the flip chip integrated circuit together forming continuous cut edges around the periphery of the flip chip, the partially cured reflowable underfill adhesive having properties suitable for reflowing during solder reflow of the solder bumps at a solder reflow temperature when the flip chip is being mounted onto a substrate so that the reflowable underfill material substantially fills the gap between the flip chip and the substrate and further cures in the gap between the flip chip and the substrate (figure 6 & 11, 65-12, 8), and wherein prior to reflow the B-staged underfill adhesive conformally surrounds the solder bumps with substantially no gap between the B-staged adhesive and the solder bumps (9, 6+; 11, 23+; & Figure 5).

Regarding claim 20, Chung teaches the underfill adhesive includes one or more of the following components: an epoxy resin (8, 52-55), a hardener, a catalyst initiator, a coloring dye, and an inorganic filler.

With respect to claim 21, Chung teaches the underfill adhesive has a coefficient of thermal expansion substantially similar to that of the substrate upon which the flip chip integrated circuit is intended to be mounted (10, 1+).

As to claims 22 and 36, Chung teaches the underfill adhesive is deposited on the active surface of the flip chip integrated circuit at a pre-cured height such that the solder bumps are at least exposed through the underfill adhesive after curing (figure 5).

In re claims 23 and 37, Chung teaches the pre-cured height of the underfill adhesive applied to the wafer ranges from 140% to 90% of the height of the solder bumps (11, 30+).

Regarding claim 24, Chung teaches the underfill adhesive layer is deposited on the active surface of the flip chip integrated circuit in wafer form before the flip chip integrated circuit is singulated from the wafer (11, 46+).

With respect to claims 25 and 38, Chung teaches the underfill adhesive is selected from the group comprising: epoxies (8, 52-55), poly-imides (8, 67-9, 1), silicone-polyimide copolymers.

As to claim 26, wherein the substrate has a plurality of contact pads, the contact pads configured to contact the solder bumps of the flip chip when the flip chip is mounted onto the substrate, the contact pads and the solder bumps forming joints electrically connecting the flip chip to the substrate (figure 6).

In re claim 35, Chung teaches an apparatus, comprising:

a semiconductor wafer having an active surface including a plurality of die formed thereon (11, 46+);

one or more bond pads [32] formed on the plurality of die;

one or more solid solder bumps [34] formed on the one or more bond pads respectively; and

a layer of B-staged underfill adhesive that is partially cured and reflowable (8, 46-52), the B-staged underfill adhesive being formed around the solder bumps on the active surface of the wafer, the reflowable underfill adhesive having properties suitable for reflowing during solder reflow of the solder bumps at a solder reflow temperature when the individual die are being mounted onto a substrate so that the reflowable underfill material substantially fills the gap between the individual die and the substrate and further cures in the gap between the flip chip and the substrate (figure 6 & 11, 65-12, 8), and wherein prior to reflow the B-staged underfill adhesive conformally surrounds the solder bumps with substantially no gap between the B-staged adhesive and the solder bumps (9, 6+; 11, 23+; & Figure 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 28-31, 33, 34, and 39-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6,399,178, as applied to claims 19 and 35 above.

Regarding claims 28 and 39, while Chung fails to teach the layer of underfill adhesive is substantially opaque thereby protecting the flip chip integrated circuit from photo induced leakage currents by blocking visible light, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the opacity through routine experimentation (MPEP 2144.05).

With respect to claims 29 and 40, while Chung fails to teach the underfill adhesive has a coefficient of thermal expansion in the range of approximately 20 x 10-6/K to approximately 30 x 10-6/K @ 25 °C, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the coefficient of thermal expansion through routine experimentation (MPEP 2144.05).

As to claims 30 and 41, while Chung fails to teach the underfill adhesive melts at between 120 to 140 degrees C and reacts at between 175 to 195 degrees C, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize

the underfill adhesive melt and reaction temperatures through routine experimentation (MPEP 2144.05).

In re claims 31 and 42, while Chung fails to teach the underfill adhesive has an elastic modulus in the range of 1 to 10 GPa, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the elastic modulus through routine experimentation (MPEP 2144.05).

With respect to claim 34, while Chung fails to teach a fluxing material is provided on the substrate, the use of conventional materials to perform their known functions is obvious (MPEP 2144.07). A skilled artisan knows that a fluxing material on the substrate would increase the bonding between the flip chip and the substrate.

As to claim 43, Chung teaches an apparatus of claim 35, further comprising:

a semiconductor wafer having an active surface including a plurality of dice formed thereon;

a plurality of bond pads formed on each of the plurality of dice;

a plurality of solder bumps, each solder bump being formed on an associated bond pad;

and

a layer of B-staged underfill adhesive that is partially cured and reflowable, the B-staged (8, 46-52) underfill adhesive [12] being formed around the solder bumps on the active surface of the wafer, the reflowable underfill adhesive having properties suitable for reflowing during solder reflow of the solder bumps at a solder reflow temperature when the individual die are being mounted onto a substrate so that the reflowable

underfill material substantially fills the gap between the individual die and the substrate and further cures in the gap between the flip chip and the substrate (9, 6+; 11, 23+; & Figure 5).

Chung fails to teach a dam around the periphery of the wafer to prevent the underfill material deposited onto the active surface of the wafer from flowing off the wafer before the partial curing of the adhesive layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a dam in the invention of Chung because the use of a dam is conventionally known in the art to skilled artisans to be used to control flow of a material. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).[30]

Rejections over Capote et al., US Patent Application Publication 2002/0014703

Claims 19-26, and 28-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over, Capote et al., US Patent Application Publication 2002/0014703.

Capote (figures 3, 5-8) teaches an apparatus, comprising:

a flip chip integrated circuit [10] having flip chip bond pads [24] with solder bumps [30] formed directly on an active surface of the flip chip; and

a substantially uniform layer of partially cured reflowable underfill adhesive [22] applied directly on the active surface of the flip chip integrated circuit and around the solder bumps formed onto the active surface, the substantially uniform layer of underfill adhesive and the flip chip integrated circuit together forming continuous cut edges

around the periphery of the flip chip (figures 3, 5-8 clearly show a continuous cut edges around the periphery of the flip chip), the partially cured reflowable underfill adhesive having properties suitable for reflowing during solder reflow of the solder bumps at a solder reflow temperature when the flip chip is being mounted onto a substrate so that the reflowable underfill material substantially fills the gap between the flip chip and the substrate and further cures in the gap between the flip chip and the substrate (4, 2+ & [0040]), and wherein prior to reflow the underfill adhesive conformally surrounds the solder bumps with substantially no gap between the adhesive and the solder bumps (Figure 7).

Capote fails to teach the underfill is B-staged.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a B-staged underfill in the invention of Capote because B-staged underfills are commonly known in the art , as evinced by Chung, US Patent 6,399,178 (8, 35+). The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Regarding claim 20, Capote teaches the underfill adhesive includes one or more of the following components: an epoxy resin, a hardener, a catalyst initiator, a coloring dye, and an inorganic filler ([0055] & [0056]).

Regarding claim 21, Capote teaches the underfill adhesive has a coefficient of thermal expansion substantially similar to that of the substrate upon which the flip chip integrated circuit is intended to be mounted [0023].

With respect to claims 22 and 36, Capote teaches the underfill adhesive is deposited on the active surface of the flip chip integrated circuit at a pre-cured height such that the solder bumps are at least exposed through the underfill adhesive after curing (figure 7).

Regarding claim 23 and 37, while Capote fails to teach the pre-cured height of the underfill adhesive applied to the wafer ranges from 140% to 90% of the height of the solder bumps, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the pre-cured height of the underfill adhesive through routine experimentation (MPEP 2144.05).

With respect to claim 24, Capote teaches the underfill adhesive layer is deposited on the active surface of the flip chip integrated circuit in wafer form before the flip chip integrated circuit is singulated from the wafer [0025].

As to claims 25 and 38, Capote teaches the underfill adhesive is selected from the group comprising: epoxies, poly-imides [0037], silicone-polyimide copolymers.

In re claim 26, Capote teaches the substrate has a plurality of contact pads, the contact pads configured to contact the solder bumps of the flip chip when the flip chip is mounted onto the substrate, the contact pads and the solder bumps forming joints electrically connecting the flip chip to the substrate (figure 3).

With respect to claims 28 and 39, while Capote fails to teach the layer of underfill adhesive is substantially opaque thereby protecting the flip chip integrated circuit from photo induced leakage currents by blocking visible light, it would have been obvious to

one ordinary skill in the art at the time of the invention to optimize the opacity of the underfill adhesive through routine experimentation (MPEP 2144.05).

As to claims 29 and 40, while Capote fails to teach the underfill adhesive has a coefficient of thermal expansion in the range of approximately 20 x 10-6/K to approximately 30 x 10-6/K @ 25 °C, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the coefficient of thermal expansion of the underfill adhesive through routine experimentation (MPEP 2144.05).

In re claims 30 and 41, while Capote fails to teach the underfill adhesive melts at between 120 to 140 degrees C and reacts at between 175 to 195 degrees C, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the melt and reaction temperatures of the underfill adhesive through routine experimentation (MPEP 2144.05).

Regarding claims 31 and 42, while Capote fails to teach the underfill adhesive has an elastic modulus in the range of 1 to 10 GPa, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the elastic modulus of the underfill adhesive through routine experimentation (MPEP 2144.05).

With respect to claim 32, while Capote fails to teach a dam around the periphery of the wafer to prevent the underfill material deposited onto the surface of the wafer from flowing off the wafer before the partial curing of the adhesive layer, the use of a dam is conventionally known in the art to skilled artisans to prevent the flowing of the underfill adhesive. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

As to claim 34, Capote teaches a fluxing material is provided on the substrate [0057].

In re claim 35, Capote teaches an apparatus, comprising:

a semiconductor wafer [0025] having an active surface including a plurality of die formed thereon;

one or more bond pads [24] formed on the plurality of die;

one or more solder bumps [30] formed on the one or more bond pads respectively; and

a layer of underfill adhesive (22) that is partially cured and reflowable, the underfill adhesive being formed around the solder bumps on the active surface of the wafer, the reflowable underfill adhesive having properties suitable for reflowing during solder reflow of the solder bumps at a solder reflow temperature when the individual die are being mounted onto a substrate so that the reflowable underfill material substantially fills the gap between the individual die and the substrate and further cures in the gap between the flip chip and the substrate (4, 2+ & [0040], and wherein prior to reflow the underfill adhesive conformally surrounds the solder bumps with substantially no gap between the adhesive and the solder bumps (Figure 7).

Capote fails to teach the underfill is B-staged.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a B-staged underfill in the invention of Capote because B-staged underfills are commonly known in the art, as evinced by Chung, US Patent 6,399,178

(8, 35+). The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

In re claim 43, Capote teaches an apparatus of claim 35, further comprising:

a semiconductor wafer having an active surface including a plurality of dice [10] formed thereon;

a plurality of bond pads [24] formed on each of the plurality of dice;

a plurality of solder bumps [30], each solder bump being formed on an associated bond pad;

and

a layer of underfill adhesive that is partially cured and reflowable, the underfill adhesive [22] being formed around the solder bumps on the active surface of the wafer, the reflowable underfill adhesive having properties suitable for reflowing during solder reflow of the solder bumps at a solder reflow temperature when the individual die are being mounted onto a substrate so that the reflowable underfill material substantially fills the gap between the individual die and the substrate and further cures in the gap between the flip chip and the substrate (Figure 7).

Capote fails to teach a dam around the periphery of the wafer to prevent the underfill material deposited onto the active surface of the wafer from flowing off the wafer before the partial curing of the adhesive layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a dam in the invention of Chung because the use of a dam is

conventionally known in the art to skilled artisans to be used to control flow of a material. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David A. Zarneke/

Primary Examiner, Art Unit 2891
8/11/08